CLAIMS

What is claimed is:

1. A method comprising:

comparing an output feedback voltage with a reference voltage to determine whether said output feedback voltage is greater than or less than said reference voltage;

responding to said comparison by either:

increasing a frequency for a clock signal if said output feedback voltage is less than said reference voltage;

decreasing said frequency for said clock signal if said output feedback voltage is greater than said reference voltage; or

disabling said clock signal if said output feedback voltage is much greater than said reference voltage; and

generating a pumped voltage in response to changes to said clock signal.

2. The method of claim 1 further comprising pumping charge from a supply voltage to generate a pumped output voltage, said pumped output voltage having a higher voltage level than said supply voltage.

3. The method of claim 2 further comprising filtering said pumped output voltage to remove noise from said pump output voltage.

4. The method of claim 3 further comprising dividing down said pump output voltage to obtain said output feedback voltage.

5. The method of claim 4 further comprising enabling said clock signal if said clock signal has been disabled and said output feedback voltage is presently less than or equal to said reference voltage.

6. The method of claim 5 wherein said clock signal comprises a four phase clocking scheme.

7. The method of claim 6 wherein a bias signal controls said clock signal, said bias signal to increase or decrease said frequency of said clock signal in response to said comparison of said output feedback voltage and said reference voltage.

8. A method comprising:

receiving a reference voltage;

receiving a feedback voltage, said feedback voltage provided from a charge pump output;

comparing said reference voltage and said feedback voltage;

adjusting operation of charge pumping in response to said comparison; and

generating a pumped voltage from said charge pumping.

9. The method of claim 8 further comprising outputting said pumped voltage at said charge pump output.

10. The method of claim 9 further comprising filtering said pumped voltage through a low threshold voltage (Vt) diode device.

11. The method of claim 10 wherein said diode device is to protect a charge pump by preventing charge from flowing from said charge pump output back into said charge pump.

12. The method of claim 11 wherein said operation adjusting further comprises frequency blocking of clocking to pump cells in said charge pump.

13. The method of claim 12 wherein said operation adjusting further comprises biasing a clock generator to alter a clock frequency of a clock signal generated from said clock generator, said clock signal to control pumping action of said pump cells.

14. The method of claim 13 wherein said biasing further comprises decreasing said clock frequency to slow down pumping action of said pump cells in order to generate a lower pumped voltage at said charge pump output.

15. The method of claim 14 wherein said biasing further comprises increasing said clock frequency to speed up pumping action of said pump cells in order to generate a high pumped voltage at said charge pump output.

16. The method of claim 15 further comprising feeding a form of said pumped

voltage from said charge pump output back as a feedback voltage for comparison with said reference voltage.

17. An apparatus comprising:

a comparator to receive and compare a reference voltage and a feedback voltage, said comparator to provide a first signal and a second signal;

a clock system coupled to said comparator, said clock system to generate clock signals in response to said first and second signals;

a pump cell coupled to said clock system, said pump cell to pump charge from a supply voltage to generate a pumped voltage greater than said supply voltage, wherein operation of said pump cell is controlled with said clock signals;

a diode device coupled to said pump cell to filter said pumped voltage, said diode device to pass charge from an output of said pump cell to a charge pump output node; and

a feedback mechanism to couple a charge pump output voltage from said charge pump output node to said comparator.

18. The apparatus of claim 17 wherein said first and second signals are generated by said comparator in response to a comparison of said reference voltage and said feedback voltage.

19. The apparatus of claim 18 wherein said first signal is an analog signal, said first signal to bias said clock system to either increase or decrease frequency of said clock signals.

20. The apparatus of claim 19 wherein said second signal is a digital signal, said second signal to frequency block said clock system to enable or disable output of said clock signals to said pump cell.

21. The apparatus of claim 20 wherein said clock system further comprises:

an oscillator coupled to said first signal and said second signal, said oscillator to generate a oscillating clock signal in response to said first signal; and

a phase clock generator coupled to said oscillator and said second signal, said phase clock generator to receive said oscillating clock signal and to generate a set of four phase clock signals based on frequency of said oscillating clock signal.

22. The apparatus of claim 21 wherein said first signal is to control said frequency of said oscillating clock signal.

23. The apparatus of claim 22 wherein said second signal is to disable operation of said oscillator and said phase clock generator if said feedback voltage is much greater than said reference voltage.

24. The apparatus of claim 23 wherein said diode device is a low threshold voltage (Vt), low pass diode.

25. The apparatus of claim 24 further comprising a voltage divider coupled to said

charge pump output node and said feedback mechanism, said voltage divider to divide said charge pump output voltage down to said feedback voltage.

26. An integrated circuit comprising:

a memory array to store data and instructions;

decoding logic coupled to said memory array, said decoding logic to decode addresses to access memory cells within said memory array; and

a charge pump coupled to said decoding logic, said charge pump to provide a high voltage supply for memory accesses, said charge pump further comprising:

a comparator to receive and compare a reference voltage and a feedback voltage, said comparator to provide a first signal and a second signal;

a clock system coupled to said comparator, said clock system to generate clock signals in response to said first and second signals;

a pump cell coupled to said clock system, said pump cell to pump charge from a supply voltage to generate a pumped voltage greater than said supply voltage, wherein operation of said pump cell is controlled with said clock signals;

a diode device coupled to said pump cell to filter said pumped voltage, said diode device to pass charge from an output of said pump cell to a charge pump output node; and

a feedback mechanism to couple a charge pump output voltage from said charge pump output node to said comparator.

27. The integrated circuit of claim 26 wherein:

said first and second signals are generated by said comparator in response to a comparison of said reference voltage and said feedback voltage;

said first signal is an analog signal, said first signal to bias said clock system to either increase or decrease frequency of said clock signals; and

said second signal is a digital signal, said second signal to frequency block said clock system to enable or disable output of said clock signals to said pump cell.

28. The integrated circuit of claim 27 wherein said clock system further comprises:

an oscillator coupled to said first signal and said second signal, said oscillator to generate a oscillating clock signal in response to said first signal, said first signal is to control said frequency of said oscillating clock signal;

a phase clock generator coupled to said oscillator and said second signal, said phase clock generator to receive said oscillating clock signal and to generate a set of four phase clock signals based on frequency of said oscillating clock signal; and

wherein said second signal is to disable operation of said oscillator and said phase clock generator if said feedback voltage is much greater than said reference voltage.

29. The integrated circuit of claim 28 further comprising a voltage divider coupled to said charge pump output node and said feedback mechanism, said voltage divider to divide said charge pump output voltage down to said feedback voltage.